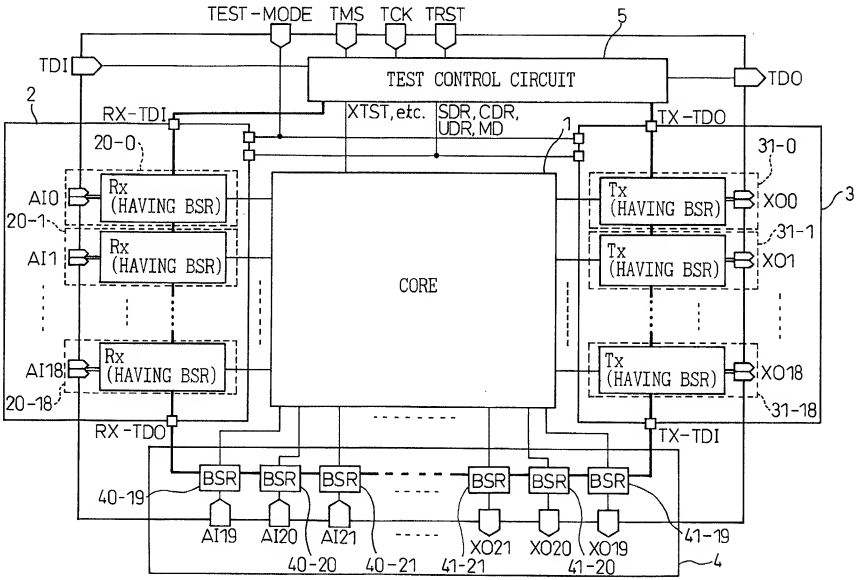
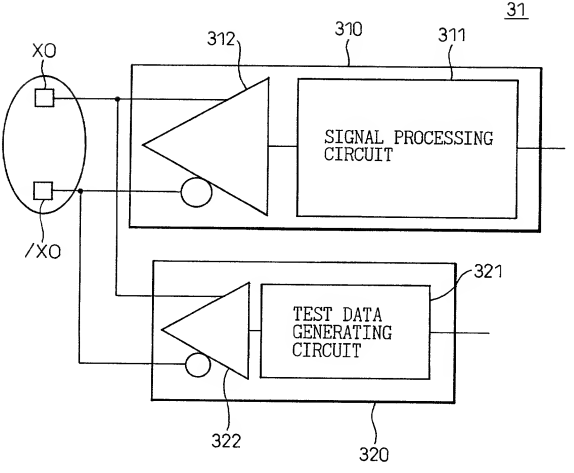
Fig.1


TEST-MODE
TMS
TCK
TRST
5
TDI
TEST CONTROL CIRCUIT
TDO
2
RX-TDI
XTST, etc.
SDR, CDR, UDR, MD
1
TX-TDO
20-0
31-0
AI0
Rx (HAVING BSR)
Tx (HAVING BSR)
XO0
3
20-1
31-1
AI1
XO1
CORE
AI18
XO18
20-18
31-18
RX-TDO
TX-TDI
BSR
40-19
41-19
AI19
AI20
AI21
XO21
XO20
XO19
40-20
40-21
41-21
41-20
4

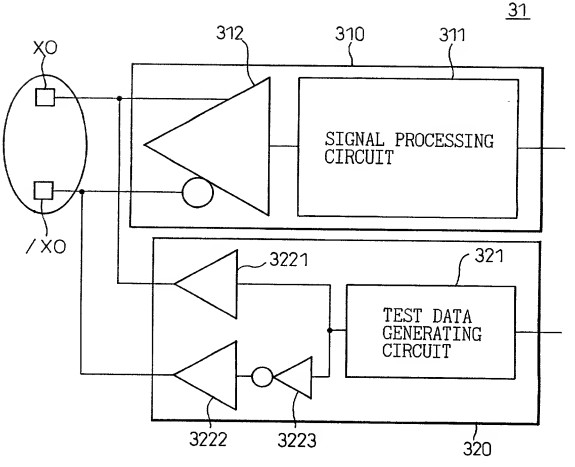
1/14

Fig.2



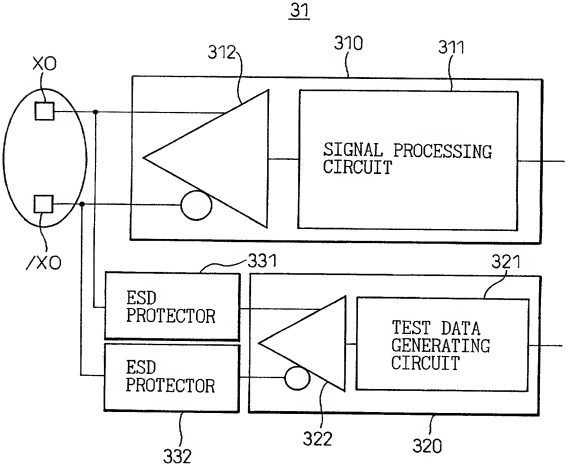
2002055-022902

Fig.3



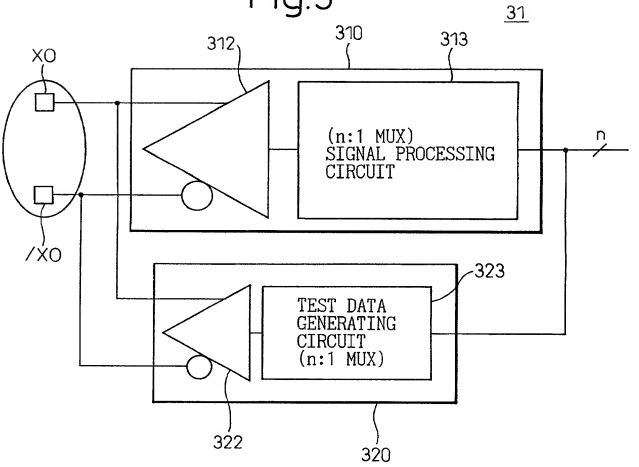
2002-0226021-0082005

Fig.4



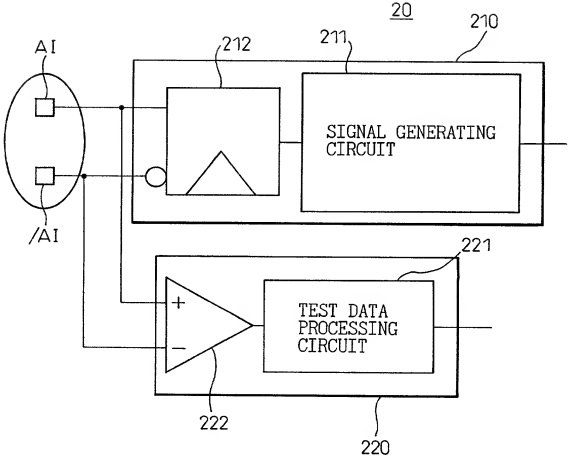
2002205028001

Fig.5



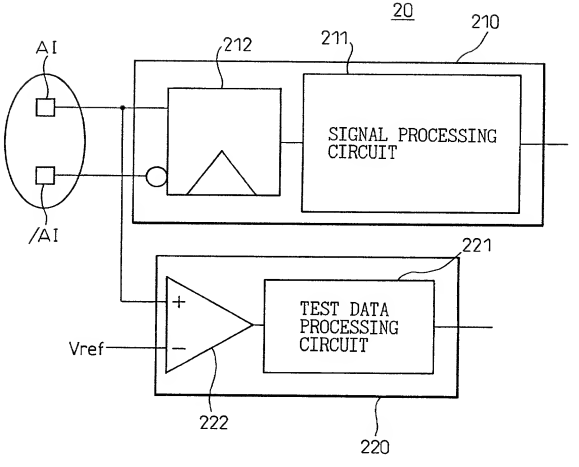
2002-550280T 10082055.022602

Fig.6



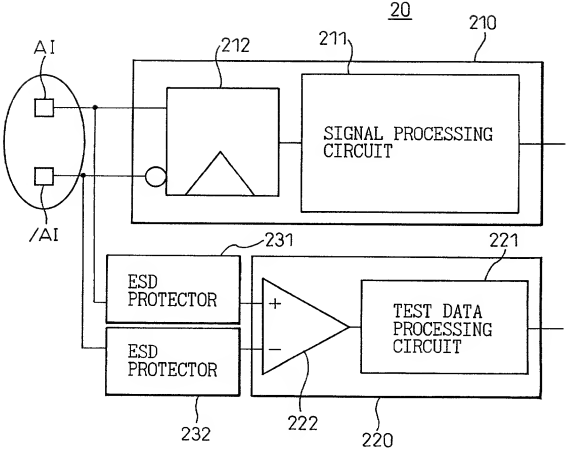
2002-0226021 10082055

Fig.7



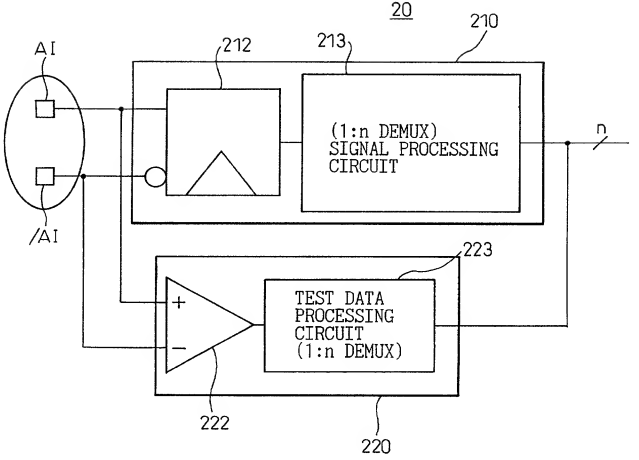
2052220.5028001

Fig.8



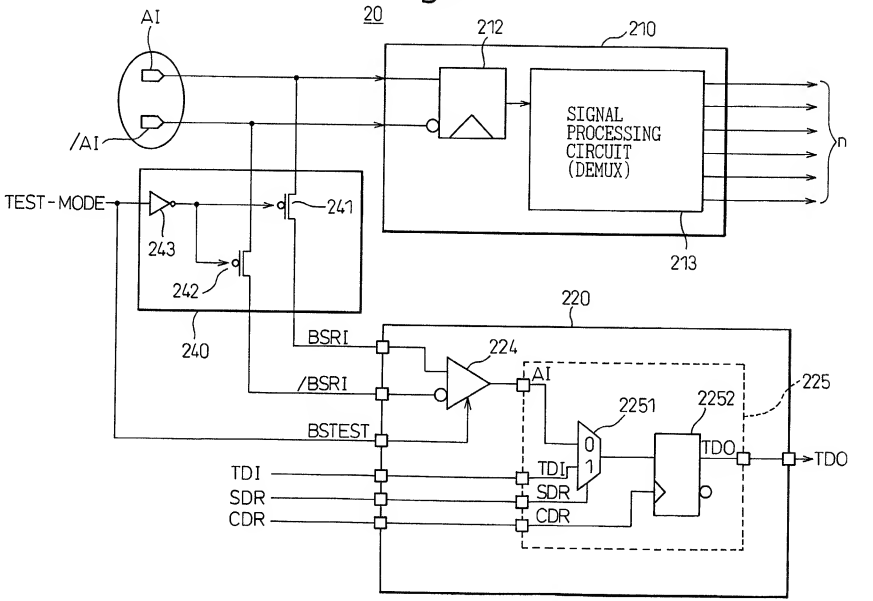
20020220.5502880D1

Fig.9



1020020055022602

Fig.10


AI
/AI
20
212
210
SIGNAL
PROCESSING
CIRCUIT
(DEMUX)
n
213
TEST-MODE
241
243
242
240
220
BSRI
/BSRI
BSTEST
224
AI
2251
2252
225
TDO
TDO
TDI
SDR
CDR
TDI
SDR
CDR
0
1

2092207 55028001

Fig.11

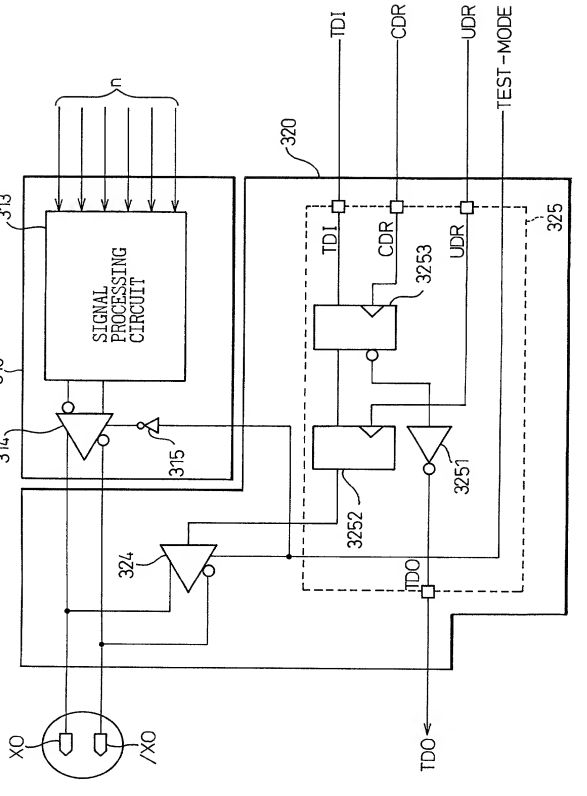


Fig.12

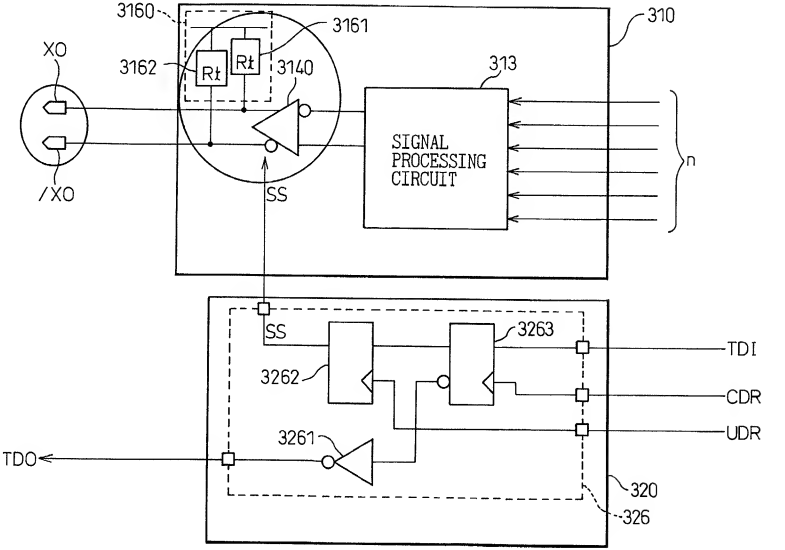
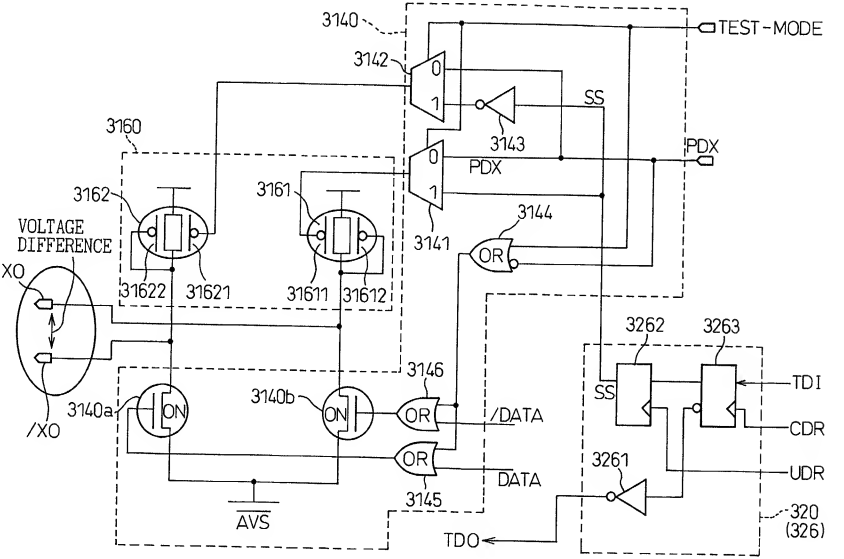

3160
3161
310
XO
3162
Rt
Rt
3140
313
SIGNAL
PROCESSING
CIRCUIT
n
/XO
SS
SS
3263
TDI
3262
CDR
UDR
3261
TDO
320
326

Fig.13


3140
TEST-MODE
3142
0
1
SS
3143
3160
PDX
0
PDX
1
3162
3161
3144
VOLTAGE
DIFFERENCE
3141
OR
XO
31622
31621
31611
31612
3262
3263
3146
TDI
SS
3140a
ON
3140b
ON
OR
/DATA
CDR
/XO
OR
3261
UDR
DATA
3145
AVS
320
(326)
TDO

2092220 "5502800T

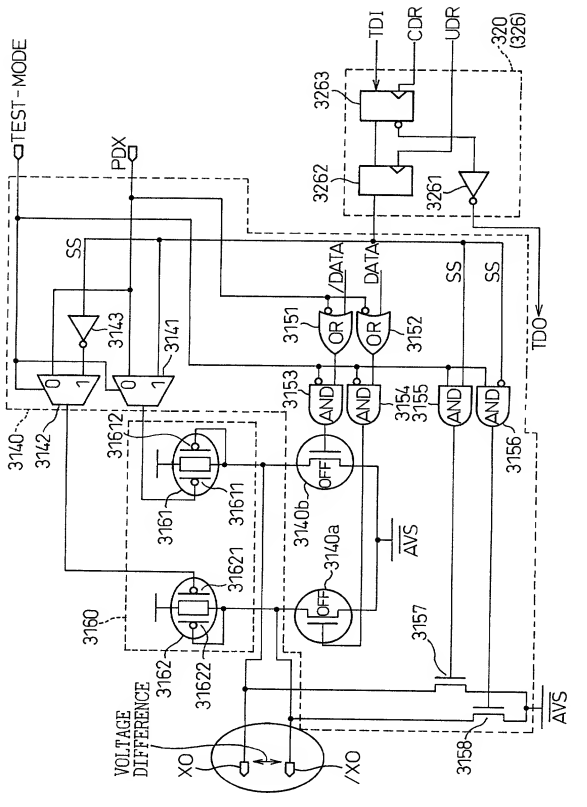



Fig.14